

## Translation of Simple Expressions

Using variables stored in registers; loading constants:

| instruction      | semantics   | intuition           |
|------------------|-------------|---------------------|
| loadc $R_i$ $c$  | $R_i = c$   | load constant       |
| move $R_i$ $R_j$ | $R_i = R_j$ | copy $R_j$ to $R_i$ |

**Script** generated by TTT

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- 51: Arithmetic Expressions

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We define the following translation schema (with  $\rho(x = a)$ ):

$$\begin{aligned} \text{code}_R^i c \rho &= \text{loadc } R_i c \\ \text{code}_R^i x \rho &= \text{move } R_i R_a \\ \text{code}_R^i x = e \rho &= \text{code}_R^i e \rho \\ &\quad \text{move } R_a R_i \end{aligned}$$

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## Translation of Expressions

Let  $\text{op} = \{\text{add}, \text{sub}, \text{div}, \text{mul}, \text{mod}, \text{le}, \text{gr}, \text{eq}, \text{leq}, \text{geq}, \text{and}, \text{or}\}$ . The R-CMa provides an instruction for each operator  $\text{op}$ .

$$\text{op } R_i R_j R_k$$

where  $R_i$  is the target register,  $R_j$  the first and  $R_k$  the second argument.

Correspondingly, we generate code as follows:

$$\text{code}_R^i e_1 \text{op } e_2 \rho = \begin{array}{l} \text{code}_R^i e_1 \rho \\ \text{code}_R^{i+1} e_2 \rho \\ \text{op } R_i R_j R_{i+1} \end{array}$$

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## Translation of Expressions

Let  $op = \{add, sub, div, mul, mod, le, gr, eq, leq, geq, and, or\}$ . The R-CMa provides an instruction for each operator  $op$ .

$$op \ R_i \ R_j \ R_k$$

where  $R_i$  is the target register,  $R_j$  the first and  $R_k$  the second argument.

Correspondingly, we generate code as follows:

$$code_R^i \ e_1 \ op \ e_2 \ \rho = \begin{array}{l} code_R^i \ e_1 \ \rho \\ code_R^{i+1} \ e_2 \ \rho \\ op \ R_i \ R_i \ R_{i+1} \end{array}$$

Example: Translate  $3*4$  with  $i = 4$ :

$$code_R^4 \ 3*4 \ \rho = \begin{array}{l} code_R^4 \ 3 \ \rho \\ code_R^5 \ 4 \ \rho \\ mul \ R_4 \ R_4 \ R_5 \end{array}$$

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## Managing Temporary Registers

Observe that temporary registers are re-used: translate  $3*4+3*4$  with  $t = 4$ :

$$code_R^4 \ 3*4+3*4 \ \rho = \begin{array}{l} code_R^4 \ 3*4 \ \rho \\ code_R^5 \ 3*4 \ \rho \\ add \ R_4 \ R_4 \ R_5 \end{array}$$

where

$$code_R^i \ 3*4 \ \rho = \begin{array}{l} loadc \ R_i \ 3 \\ loadc \ R_{i+1} \ 4 \\ mul \ R_i \ R_i \ R_{i+1} \end{array}$$

we obtain

$$code_R^4 \ 3*4+3*4 \ \rho =$$

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where  $R_i$  is the target register,  $R_j$  the first and  $R_k$  the second argument.

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## Managing Temporary Registers

Observe that temporary registers are re-used: translate  $3*4+3*4$  with  $t = 4$ :

$$code_R^4 \ 3*4+3*4 \ \rho = \begin{array}{l} code_R^4 \ 3*4 \ \rho \\ code_R^5 \ 3*4 \ \rho \\ add \ R_4 \ R_4 \ R_5 \end{array}$$

where

$$code_R^i \ 3*4 \ \rho = \begin{array}{l} loadc \ R_i \ 3 \\ loadc \ R_{i+1} \ 4 \\ mul \ R_i \ R_i \ R_{i+1} \end{array}$$

we obtain

$$code_R^4 \ 3*4+3*4 \ \rho = \begin{array}{l} loadc \ R_4 \ 3 \\ loadc \ R_5 \ 4 \\ mul \ R_4 \ R_4 \ R_5 \\ loadc \ R_5 \ 3 \\ loadc \ R_6 \ 4 \\ mul \ R_5 \ R_5 \ R_6 \\ add \ R_4 \ R_4 \ R_5 \end{array}$$

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## Semantics of Operators

The operators have the following semantics:

|                   |                                                                                                          |
|-------------------|----------------------------------------------------------------------------------------------------------|
| add $R_i R_j R_k$ | $R_i = R_j + R_k$                                                                                        |
| sub $R_i R_j R_k$ | $R_i = R_j - R_k$                                                                                        |
| div $R_i R_j R_k$ | $R_i = R_j / R_k$                                                                                        |
| mul $R_i R_j R_k$ | $R_i = R_j * R_k$                                                                                        |
| mod $R_i R_j R_k$ | $R_i = \text{signum}(R_k) \cdot k$ with<br>$ R_j  = n \cdot  R_k  + k \wedge n \geq 0, 0 \leq k <  R_k $ |
| le $R_i R_j R_k$  | $R_i = \text{if } R_j < R_k \text{ then } 1 \text{ else } 0$                                             |
| gr $R_i R_j R_k$  | $R_i = \text{if } R_j > R_k \text{ then } 1 \text{ else } 0$                                             |
| eq $R_i R_j R_k$  | $R_i = \text{if } R_j = R_k \text{ then } 1 \text{ else } 0$                                             |
| leq $R_i R_j R_k$ | $R_i = \text{if } R_j \leq R_k \text{ then } 1 \text{ else } 0$                                          |
| geq $R_i R_j R_k$ | $R_i = \text{if } R_j \geq R_k \text{ then } 1 \text{ else } 0$                                          |
| and $R_i R_j R_k$ | $R_i = R_j \& R_k$ // bit-wise and                                                                       |
| or $R_i R_j R_k$  | $R_i = R_j   R_k$ // bit-wise or                                                                         |

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## Translation of Unary Operators

Unary operators  $\text{op} = \{\text{neg}, \text{not}\}$  take only two registers:

$$\text{code}_R^i \text{ op } e \rho = \text{code}_R^i e \rho$$

$\text{op } R_i R_i$

**Note:** We use the same register.



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## Semantics of Operators

The operators have the following semantics:

|                   |                                                                                                          |
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| add $R_i R_j R_k$ | $R_i = R_j + R_k$                                                                                        |
| sub $R_i R_j R_k$ | $R_i = R_j - R_k$                                                                                        |
| div $R_i R_j R_k$ | $R_i = R_j / R_k$                                                                                        |
| mul $R_i R_j R_k$ | $R_i = R_j * R_k$                                                                                        |
| mod $R_i R_j R_k$ | $R_i = \text{signum}(R_k) \cdot k$ with<br>$ R_j  = n \cdot  R_k  + k \wedge n \geq 0, 0 \leq k <  R_k $ |
| le $R_i R_j R_k$  | $R_i = \text{if } R_j < R_k \text{ then } 1 \text{ else } 0$                                             |
| gr $R_i R_j R_k$  | $R_i = \text{if } R_j > R_k \text{ then } 1 \text{ else } 0$                                             |
| eq $R_i R_j R_k$  | $R_i = \text{if } R_j = R_k \text{ then } 1 \text{ else } 0$                                             |
| leq $R_i R_j R_k$ | $R_i = \text{if } R_j \leq R_k \text{ then } 1 \text{ else } 0$                                          |
| geq $R_i R_j R_k$ | $R_i = \text{if } R_j \geq R_k \text{ then } 1 \text{ else } 0$                                          |
| and $R_i R_j R_k$ | $R_i = R_j \& R_k$ // bit-wise and                                                                       |
| or $R_i R_j R_k$  | $R_i = R_j   R_k$ // bit-wise or                                                                         |

**Note:** all registers and memory cells contain operands in  $\mathbb{Z}$

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$$\text{code}_R^i \text{ op } e \rho = \text{code}_R^i e \rho$$

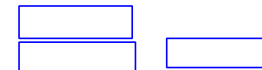
$\text{op } R_i R_i$

**Note:** We use the same register.

**Example:** Translate  $-4$  into  $R_5$ :

$$\text{code}_R^5 -4 \rho = \text{loadc } R_5 4$$

$\text{neg } R_5 R_5$



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